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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/702,112

10/30/2000

Michael Gottlieb Jensen

MIPS:0101.00US

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11/14/2003

EXAMINER

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ART UNIT

PAPER NUMBER

2183

6
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/702,112

Applicant(s)

JENSEN ET AL.

Examiner

Richard Ellis

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4-5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

1. Claims 1-35 are presented for examination.
2. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

3. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.
4. Claims 1-35 are rejected under 35 USC § 103 as being unpatentable over Larsen et al., U.S. Patent 5,115,500, in view of Heene et al., U.S. Patent 4,802,119.

Larsen et al. was cited as a prior art reference in applicant's information disclosure statement received October 30, 2000, paper number 4.

Larsen et al. taught (e.g. see figs. 1a-6) the invention substantially as claimed (as per claim 1), including a data processing ("DP") system comprising:

- 4.1. Instruction set architecture (ISA) selection logic (fig. 2) within a CPU (figs. 1a, 1b) for selecting an ISA decoding mode for a program instruction from a plurality of ISA decoding modes (col. 2 lines 8-15), the program instruction retrieved from an address (fig. 1a, 3, "IAR") in an address space of the CPU (2), the selection logic comprising;
 - 4.2. a boundary address register (fig. 2, 10) for storing boundary addresses (fig. 2, "HIGH-ORDER THREE ADDRESS BITS...") that partition the address space into a plurality of address ranges (col. 2 lines 25-29) corresponding to the plurality of ISA decoding modes (col. 2 lines 27-29); and,
 - 4.3. ISA mode selection logic, coupled to said plurality of boundary address registers, for receiving the address, and for comparing the address to said boundary addresses to determine the ISA decoding mode for the program instruction (fig. 2, 10, 8, 5).
5. Larsen et al. did not disclose a plurality of boundary address registers for storing boundary addresses, instead disclosing as his exemplary embodiment a predefined allocation of address partitions to ISA decoding modes. However, Larsen et al. did indicate that it would have been obvious to modify his system to support a plurality of runtime programmable

boundary address registers (col. 2 lines 28-35). Larsen et al. indicated that an alternate was to maintain a "table or map ... of the locations in storage and the format type of instruction that is contained therein". Heene et al. disclosed a system containing a plurality of boundary address registers for sensing and enabling an alternate operating mode upon use of an address within the range of one of the boundary address registers (fig. 4, col. 6 line 46 to col. 7 line 42). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Heene et al.'s plural boundary address register system with Larsen et al.'s system because Larsen et al. indicated at col. 2 lines 28-35 that an obvious modification of his system was the use of a "table or map" to relate address boundaries to ISA modes and Heene et al. teaches how to implement just such a "table or map" system to which Larsen et al. refers.

6. As to claim 2, Larsen et al. taught that the CPU executed a multiple-ISA application program (col. 2 lines 8-15).
7. As to claim 3, Larsen et al. taught that the multi-ISA application program comprised program components having program instructions corresponding to the plurality of ISA decoding modes (col. 4 line 56 to col. 5 line 2).
8. As to claim 4, Larsen et al. taught that the program instructions that correspond to a first ISA decoding are located within a first one of said plurality of address ranges (col. 6 lines 30-39).
9. As to claim 5, Heene et al. taught that each of the plurality of boundary address registers stored a boundary address for a corresponding address range (col. 7 lines 16-43).
10. As to claim 6, Heene et al. taught that the boundary address comprised a lower address boundary for the corresponding one of the plurality of address ranges (col. 7 lines 15-33 and 43-55).
11. As to claim 7, Heene et al. taught that the ISA mode selection logic determined that a particular boundary address register corresponded to one of the plurality of address ranges within which said address was located (fig. 4, 50, 55, 60, 65).
12. As to claim 8, Larsen et al. taught that the ISA mode selection logic selected the ISA decoding mode corresponding to a particular boundary address register (col. 6 lines 25-40).
13. As to claim 9, Larsen et al. taught that the ISA mode selection logic provided the ISA

decoding mode to the instruction decoding logic to enable correct decoding of the program instruction (fig. 2, 10, 6, 5, (col. 6 lines 3-24).

14. As to claims 10-35, they do not teach or define above the invention claimed in claims 1-9 and are therefore rejected under Larsen et al. in view of Heene et al. for the same reasons set fourth in the rejection of claims 1-9, supra. As to claims 24-29 and 34-35, official notice is taken of the fact that modern processor design occurs via the use of computer program code which describes the structure and intended operation of a processor (e.g., the well known VHDL design language) and therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have designed a system based upon the teachings of Larsen et al. and Heene et al. using such computer program code because of the well known advantages of ease of design and ease of revision/correction of the design as the process of designing the processor progresses. As to claims 34-35, such program code (e.g., VHDL) will be transmitted both within and externally of a design computer to either other computers to allow a design team to concurrently work on the design, to storage systems for storage of the design, and to computer controlled layout machinery for actual creation of the resultant silicon chip once the designers work is complete, and therefore, will, in many instances, will have been embodied in a "transmission medium".

15. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.


16. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
November 12, 2003


RICHARD L. ELLIS
PRIMARY EXAMINER